CLAIMS

1. A static random access memory (SRAM) cell having a true node and a complement node, comprising:

a continuous bit_line coupled to the complement node of the SRAM cell;

a true local bit_line coupled to the true node of the SRAM cell that is at least configured to be driven inversely to the write true_bit line;

a first and second positive field effect transistor (PFET);

a precharge line coupled to the gate of the first PFET;

a write true bit_line coupled to the gate of the second PFET; and

a negative field effect transistor (NFET) coupled to the write true bit_line through the gate of the NFET.

2. An SRAM cell having a true node and a complement node, comprising:

a continuous bit_line coupled to the complement node of the SRAM cell;

a true local bit_line coupled to the true node of the SRAM cell;

a first and second positive field effect transistor (PFET);

a precharge line coupled to the gate of the first PFET;

a write true bit_line coupled to the gate of the second PFET;

a negative field effect transistor (NFET) coupled to the write true bit_line through the gate of the NFET ~~The SRAM cell of Claim 1~~, wherein the drain of the NFET is coupled to the source of the second PFET.

3. The SRAM cell of Claim 1, wherein the continuous bit_line is coupled to an output of a NAND gate.

4. The SRAM cell of Claim 3, further comprising a write enable input coupled to an input of the NAND gate.

5. The SRAM cell of Claim 3, further comprising a data input coupled to an input of the NAND gate.

6. The SRAM cell of Claim 1, further comprising an output of a NOR gate coupled to the write true bit_line.

7. The SRAM cell of Claim 1, wherein the source of the NFET is coupled to electrical ground.

8. ~~The SRAM cell of Claim 1~~An SRAM cell having a true node and a complement node, comprising:

a continuous bit_line coupled to the complement node of the SRAM cell;

a true local bit_line coupled to the true node of the SRAM cell;

a first and second positive field effect transistor (PFET), wherein the local true bit_line is coupled to the source of the first PFET;

a precharge line coupled to the gate of the first PFET;

a write true bit_line coupled to the gate of the second PFET;

a negative field effect transistor (NFET) coupled to the write true bit_line through the gate of the NFET.

9. A method of reading indicia from an SRAM cell, comprising:

generating a low value on a write true line;

generating a high value on a continuous bit_line[[ ]]; and

evaluating the true node of the SRAM cell, wherein the true node is inverse of write true signal.

10. The method of Claim 9, further comprising transitioning a wordline value from a low value to a high value.

11. The method of Claim 9, further comprising conveying indicia from the true node of the SRAM cell to a global bitline.

12. The method of Claim 9, further comprising a step of inputting a high value into a write enable line.

13. The method of Claim 12, further comprising inverting a signal from the write enable line.

14. (Original) A method for writing indicia to a SRAM cell, comprising:
transitioning a write enable signal;
inputting data through a data in line;
generating a write true bit_line signal;
generating a complementary continuous bit_line signal;
driving the true node of the SRAM high if the write true signal is low; and
driving the true node of the SRAM low if the write true signal is high.

15. (Original) The method of Claim 14, further comprising not transitioning a precharge value associated with the precharge line.

16. (Original) The method of Claim 14, wherein a PFET directly coupled to the precharge line through the gate of the PFET does not transition from on and off.

17. (Original) The method of Claim 14, wherein the step of driving the true node of the SRAM low further comprises turning on an NFET coupled to the true node and turning off a PFET coupled to the true node.

18. (Original) The method of Claim 14, wherein the step of driving the true node of the SRAM high further comprises turning on a PFET coupled to the true node and turning off an NFET coupled to the true node.

19. A computer program product for reading indicia from an SRAM cell, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for generating a low value on a write true line;

computer code for generating a high value on a continuous bit line; and

computer code for evaluating the true node of the SRAM cell, wherein the true node is inverse of write true signal.

20. A processor for reading indicia from an SRAM cell, the processor including a computer program comprising:

computer code for generating a low value on a write true line;

computer code for generating a high value on a continuous bit_line; and

computer code for evaluating the true node of the SRAM cell, wherein the true node is inverse of write true signal.